intel®

2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - — 2716-1: 350 ns Max
  - — 2716-2: 390 ns Max
  - — 2716:   450 ns Max
- **Single + 5V Power Supply**
- **Low Power Dissipation**
  - — Active Power: 525 mW Max
  - — Standby Power: 132 mW Max

- **Pin Compatible to Intel "Universal Site" EPROMs**
- **Simple Programming Requirements**
  - — Single Location Programming
  - — Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible During Read and Program**
- **Completely Static**

The Intel 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single-address programming. It makes designing with EPROMs fast, easy and economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with high-performance + 5V microprocessors such as Intel's 8085 and 8086. Selected 2716-5s and 2716-6s are also available for slower speed applications. The 2716 also has a static standby mode which reduces power consumption without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 uses a simple and fast method for programming—a single TTL-level pulse. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Programming of any location at any time—either individually, sequentially or at random is possible with the 2716's single-address programming. Total programming time for all 16,384 bits is only 100 seconds.
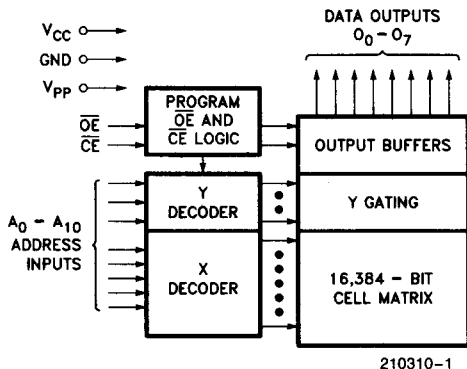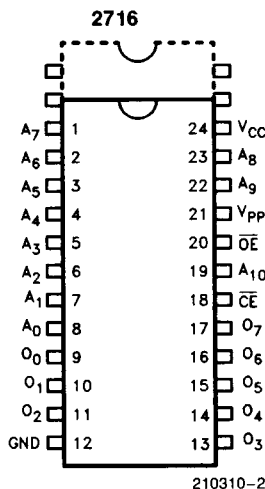
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Figure 1. Block Diagram

Pin Names

A_0-A_{10}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0-O_7	Outputs

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27512 27C512	27256 27C256	27128A 27C128	2764A 27C64 87C64	2732A
A_{15}	V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

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         _____
A7  [ 1              24 ] Vcc
A6  [ 2              23 ] A8
A5  [ 3              22 ] A9
A4  [ 4              21 ] Vpp
A3  [ 5              20 ] OE
A2  [ 6              19 ] A10
A1  [ 7              18 ] CE
A0  [ 8              17 ] O7
O0  [ 9              16 ] O6
O1  [ 10             15 ] O5
O2  [ 11             14 ] O4
GND [ 12             13 ] O3
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2732A	2764A 27C64 87C64	27128A 27C128	27256 27C256	27512 27C512
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A_{14}	A_{14}
V_{CC}	N.C.	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ / $\overline{ALE/CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2716 pins.

Figure 2. Cerdip Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
I	−40°C to +85°C	44

EXPRESS OPTIONS

2716 Versions

Packaging Options	
Speed Versions	Cerdip
−1	Q
STD	Q, I

DEVICE OPERATION

The six modes of operation of the 2716 are listed in Table 1. It should be noted that inputs for all modes are TTL levels. The power supplies required are a $+5V$ V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The 2716 has a standby mode which reduces the maximum active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because 2716s are usually used in larger memory arrays, Intel has provided a 2-line control function that accommodates this use of multiple memory connections. The two-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 18) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low-power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active-high, TTL program pulse is applied to the $\overline{CE}$ input. A pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	$+5$	$+5$	D_{OUT}
Output Disable	V_{IL}	V_{IH}	$+5$	$+5$	High Z
Standby	V_{IH}	X	$+5$	$+5$	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	$+25$	$+5$	D_{IN}
Verify	V_{IL}	V_{IL}	$+25$	$+5$	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	$+25$	$+5$	High Z

NOTE:
1. X can be V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . − 10°C to + 80°C

Storage Temperature . . . . − 65°C to + 125°C

All Input or Output Voltages with

Respect to Ground . . . . + 6V to − 0.3V

V_{PP} Supply Voltage with Respect

to Ground During Program . . . . . + 26.5V to − 0.3V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	2716	2716-1	2716-2
Temperature Range	0°C–70°C	0°C–70°C	0°C–70°C
V_{CC} Power Supply[1, 2]	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply[2]	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ[3]	Max		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = − 400 μA

A.C. CHARACTERISTICS

Symbol	Parameter	Limits (ns)						Test Conditions†
		2716		2716-1		2716-2		
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		450		350		390	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390	$\overline{OE}$ = V_{IL}
t_{OE}[4]	Output Enable to Output Delay		120		120		120	$\overline{CE}$ = V_{IL}
t_{DF}[4, 6]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	100	0	100	0	100	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2716s.

Program Inhibit

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL-level program pulse applied to a 2716's $\overline{CE}$ input with V_{PP} at 25V will program that 2716. A low-level $\overline{CE}$ input inhibits the other 2716 from being programmed.

Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room-level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Ws/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure.

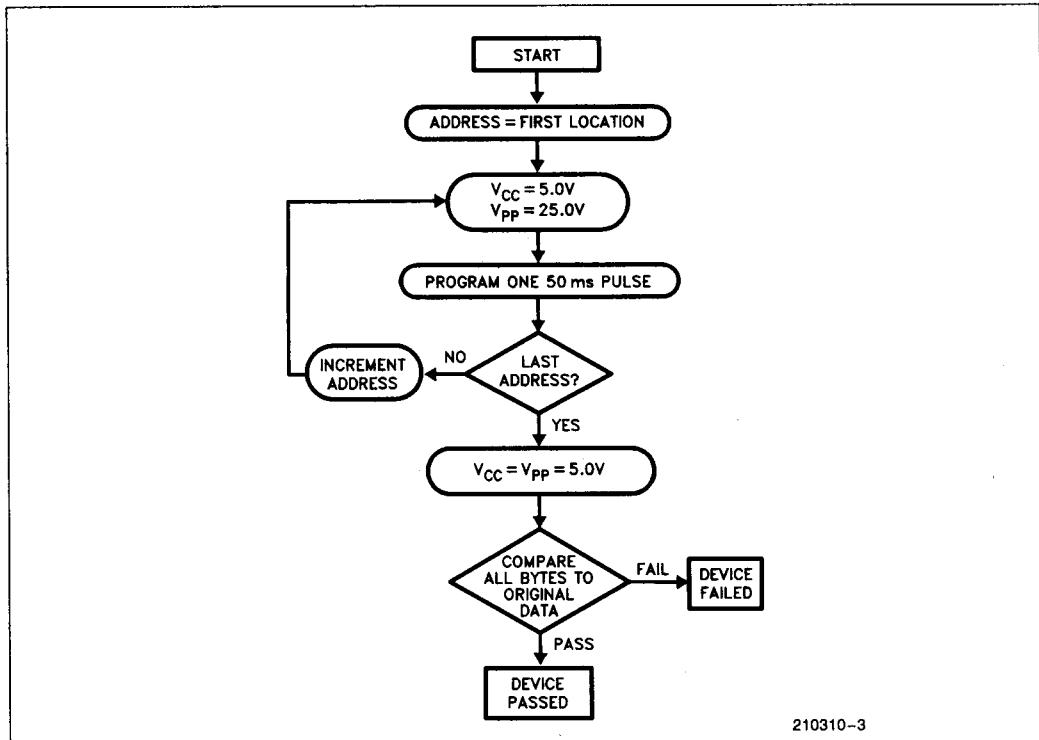**Figure 3. Standard Programming Flowchart**

CAPACITANCE[4] $T_A = 25°C, f = 1$ MHz

Symbol	Parameter	Typ[3]	Max	Unit	Test Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

†A.C. TEST CONDITIONS

Output Load . . . . 1 TTL gate and
C_L = 100 pF

Input Rise and Fall Times . . . . ≤ 20 ns

Input Pulse Levels . . . . 0.8V to 2.2V

Timing Measurement Reference Level:
  Inputs . . . . 0.8V and 2V
  Outputs . . . . 0.8V and 2V

A.C. WAVEFORMS[1]
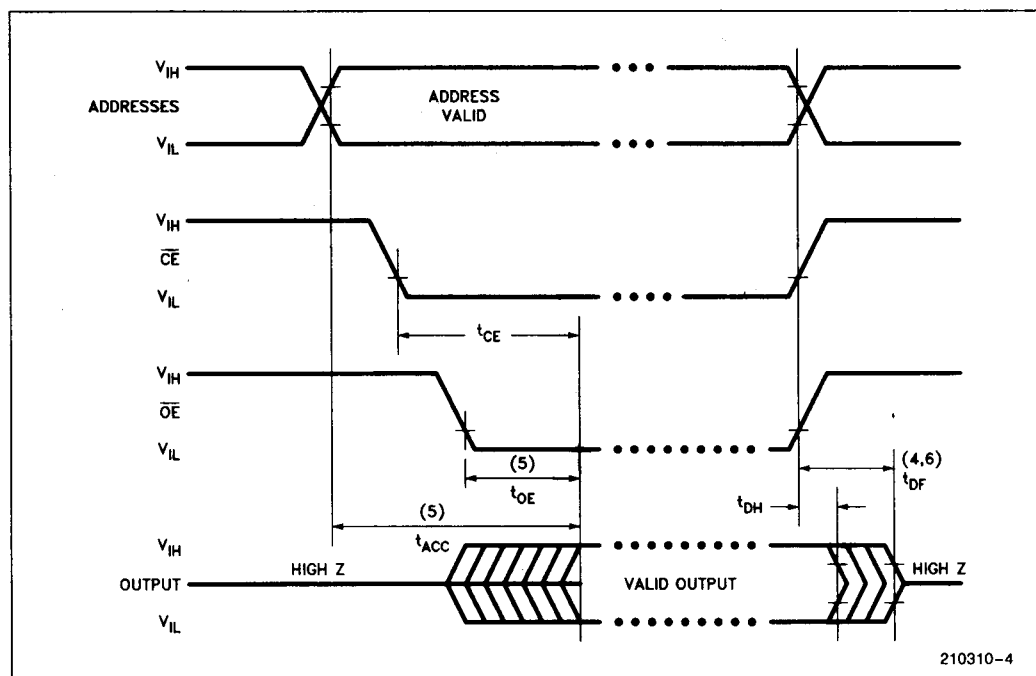
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NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING CHARACTERISTICS

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$, $V_{CC}^{(1)} = 5V \pm 5\%$, $V_{PP}^{(1, 2)} = 25V \pm 1V$

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	$V_{IN} = 5.25V/0.45$
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE} = V_{IL}$
I_{PP2}	V_{PP} Supply Current during Programming Pulse			30	mA	$\overline{CE} = V_{IH}$
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	−0.1		0.8	V	
V_{IH}	Input High Level	2.0		$V_{CC} + 1$	V	

A.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$, $V_{CC}^{(1)} = 5V \pm 5\%$, $V_{PP}^{(1, 2)} = 25V \pm 1V$

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions*
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		200	ns	$\overline{CE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			200	ns	$\overline{CE} = V_{IL}$
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

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*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns

Input Pulse Levels . . . . 0.8V to 2.2V

Input Timing Reference Level . . . . 0.8V and 2V

Output Timing Reference Level . . . . 0.8V and 2V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716 must not be inserted into or removed from a board with V_{PP} at 25 $\pm 1V$ to prevent damage to the device.
2. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is $+26V$. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

PROGRAMMING WAVEFORMS
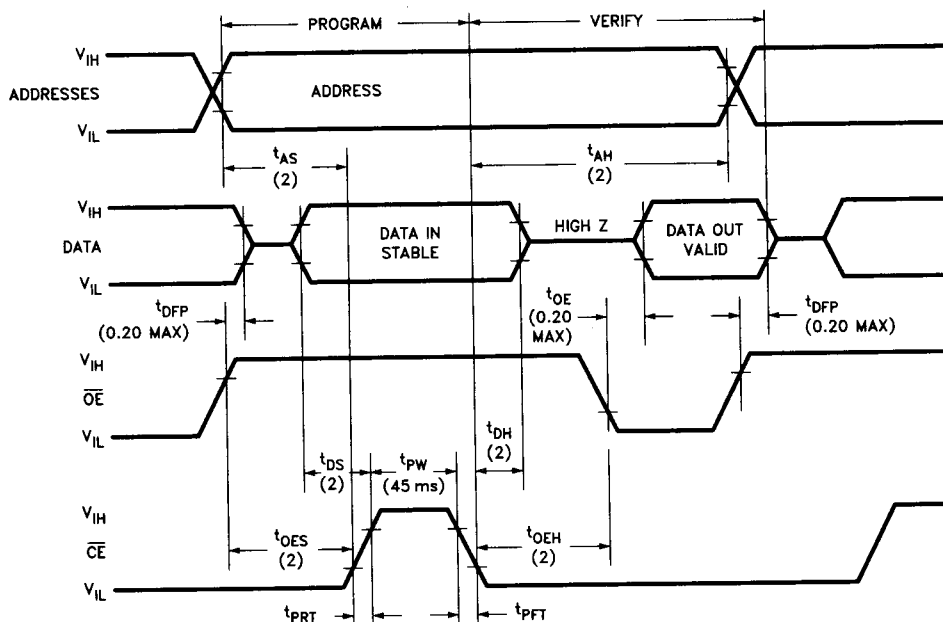
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NOTES:
1. All times shown in parenthesis are minimum times and are μs unless otherwise noted.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

REVISION HISTORY

Number	Description
03	Deleted -5 and -6 speed bins. Added Express options. Added Standard Programming Flowchart. Revised Pin Configuration and Block Diagram.