

■ MBM27128-20, MBM27128-25, MBM27128-30

UV Erasable 131,072-Bit
Read Only Memory

Description

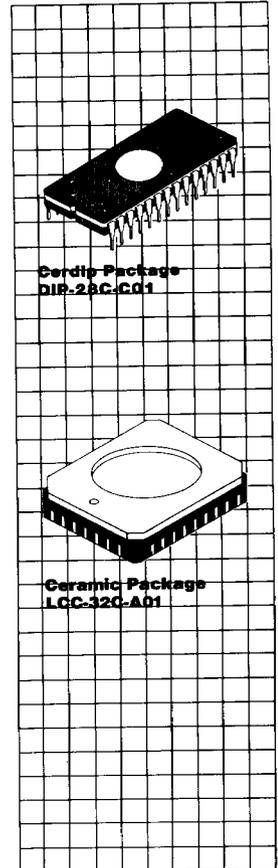
The Fujitsu MBM27128 is a high speed 131,072-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package or leadless chip carrier (32-pin) with a transparent lid is used to package the MBM27128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27128 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in single supply systems.

Features

- Organized as 16,384 x 8 fully decoded
- Low power requirement: [550 mW (act), 193 mW (standby)]
- No clocks required (fully static operation)
- Programmable utilizing the Quick Pro™ Algorithm
- Program compatible with the Intel Intelligent Programming™ Algorithm
- Fast Access Time:
 - MBM27128-20 200 ns max.
 - MBM27128-25 250 ns max.
 - MBM27128-30 300 ns max.
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Output Enable \bar{G} pin provides precise control of the data bus
- Single +5V operation
- Standard 28-pin DIP package
- Pin compatible with Intel 27128



**Serdip Package
DIP-28C-G01**

**Ceramic Package
LCC-32C-A01**

Quick Pro™ is a trademark of Fujitsu Microelectronics Inc.
intelligent Programming™ is a trademark of Intel Corporation.

MBM27128-20
MBM27128-25
MBM27128-30

Capacitance
($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance ($V_{IN} = 0\text{V}$)	C_{IN}	—	4	6	pF
Output Capacitance ($V_{OUT} = 0\text{V}$)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	$V_{CC} - 0.6$	—	$V_{CC} + 0.6$	V	
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 1$	V	
Input Low Voltage	V_{IL}	-0.1	—	0.8	V	

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current ($V_{IN} = 5.5\text{V}$)	I_{LI}	—	—	10	μA
Output Leakage Current ($V_{OUT} = 5.5\text{V}$)	I_{LO}	—	—	10	μA
V_{CC} Standby Current ($\bar{E} = V_{IH}$)	I_{CC1}	—	—	35	mA
V_{CC} Supply Current ($\bar{E} = V_{IL}$)	I_{CC2}	—	—	100	mA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6\text{V}$)	I_{PP}	—	—	5	mA
Output Low Voltage ($V_{OL} = 2.1\text{mA}$)	V_{OL}	—	—	0.45	V
Output High Voltage ($I_{OH} = -400\mu\text{A}$)	V_{OH}	2.4	—	—	V

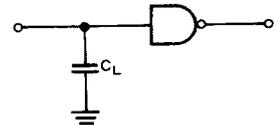
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Alternate	Standard*	MBM27128-20		MBM27128-25		MBM27128-30		Unit
				Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}	TAVQV		200		250		300		ns
\bar{E} to Output Delay	t_{CE}	TELQV		200		250		300		ns
\bar{G} to Output Delay	t_{OE}	TGLQV		70		100		120		ns
Address to Hold Time	t_{OH}	TAXQX		0	0	0	0			ns
\bar{E} or \bar{G} High to Output Float	t_{DF}	TGHQZ, TEHQZ		0	60	0	60	0	105	ns

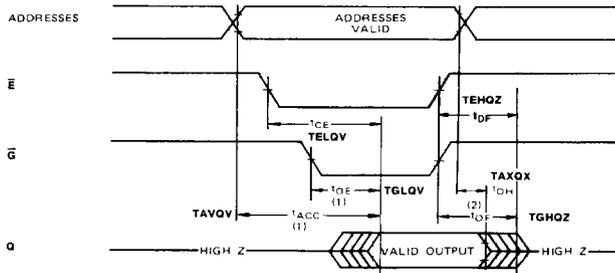
AC Test Conditions
(Including programming)

Input Pulse levels:
Input Rise and Fall Time:
Timing Measurement Reference Levels:
Output Load:

0.8V to 2.2V
 $\leq 20\text{nsec}$
1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
1 TTL gate and $C_L = 100\text{pF}$



Operation Timing Diagram



Note 1. \bar{G} may be delayed up to TAVQV-TGLQV after falling edge of \bar{E} without impact on TAVQV.
Notes 2. TGHQZ or TEHQZ is specified from \bar{G} or \bar{E} respectively, whichever ever occurs first.

Programming/Erasing Information

Memory Cell Description

The MBM27128 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27128 has all 131,072-bits in the "1" or high state. "0"s are loaded into the MBM27128

through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and \bar{E} and \bar{P} are both at V_{IL} . During programming, \bar{E} is kept at V_{IL} . A 0.1 μ F capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both

the address and data are stable, 50 msec, TTL low level pulse is applied to the \bar{P} input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the \bar{P} input is prohibited when programming.

Fig. 1 — Memory Cell

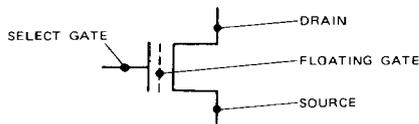
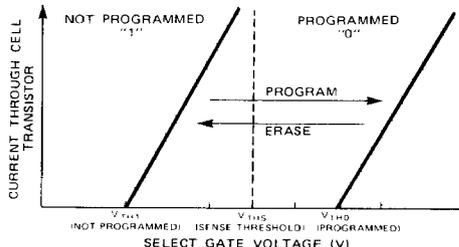


Fig. 2 — Memory Cell Threshold Shift



**Programming/Erase
 Information, continued**

“Quick Pro™” Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input and a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach sufficient stored charge levels.

Erase

In order to clear all locations of their programmed contents,

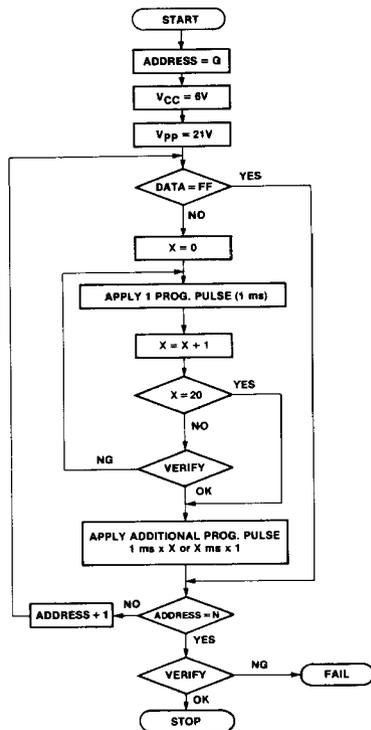
it is necessary to expose the MBM27128 to an ultraviolet light source. A dosage of 15W-seconds/cm² is required to completely erase an MBM27128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000µW/cm² for 15 to 20 minutes. The MBM27128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

MBM27128 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27128 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

It is important to note that the

Figure 3. — Quick Pro™ Flow Chart

V_{CC} = 6V ± 0.25V
 V_{PP} = 21V ± 0.5V
 T_{pw} = 1 ms ± 50µs
 (* = X ms ± 5%)
 G: START ADDRESS
 N: STOP ADDRESS
 MAXIMUM 40 ms + α/BYTE
 MINIMUM 2 ms + α/BYTE
 (FOR EXAMPLE
 64K BIT EPROM
 MAXIMUM 320µsec + β
 MINIMUM 15µsec + β)

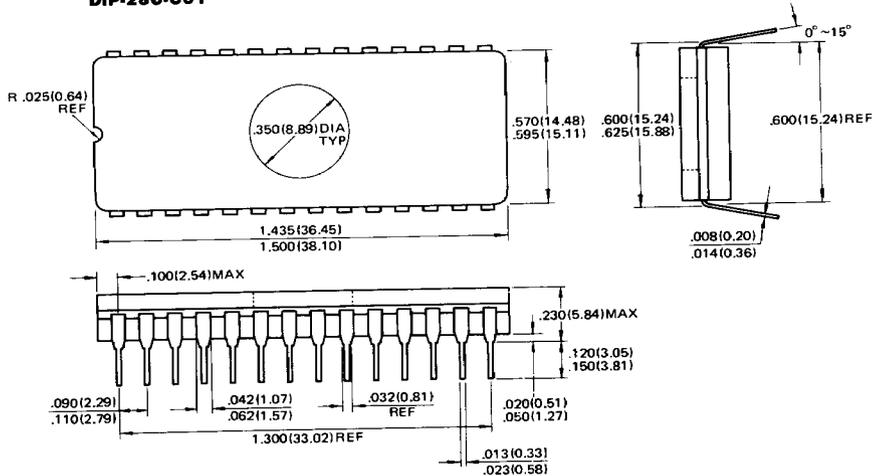


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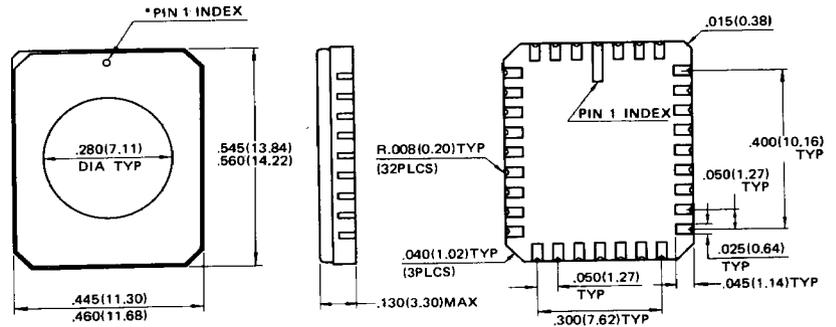
MBM27128-20
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Package Dimensions
 Dimensions in inches
 (millimeters)

**28-Lead Cerdip
 (With Transparent Lid)
 Dual In-Line Package
 DIP-28C-C01**



**32-Pin Leadless Chip Carrier
 LCC-32C-A01**



*Shape of Pin 1 index: Subject to change without notice