4096 x 8 Static Read Only Memory

SY2332/33

SYNERTEK
A SUBSIDIARY OF HONEYWELL

MEMORY PRODUCTS

- SY2333-2732 EPROM Pin Compatible
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time—450ns (max)
- Totally Static Operation
- Completely TTL Compatible
- SY2332-2532 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- 2708/2716/2532/2732 EPROMs Accepted as Program Data Inputs

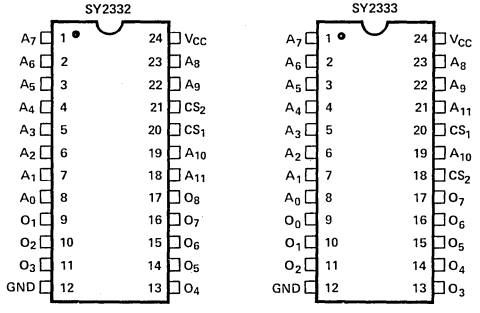
ROMs

The SY2332/3 high performance read only memory is organized 4096 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

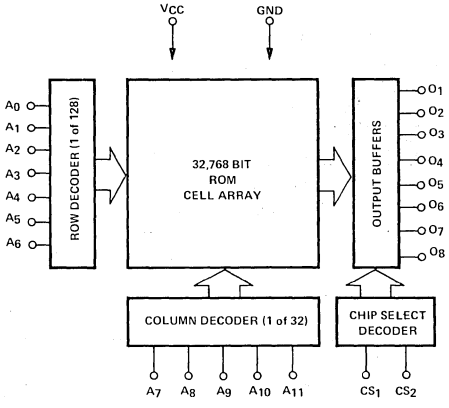
The SY2332/3 operates totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace either the 2732 or 2532 32K EPROMs, the SY2332/3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2333	Cerdip	450ns	0°C to +70°C
SYP2333	Plastic	450ns	0°C to +70°C
SYD2332	Cerdip	450ns	0°C to +70°C
SYP2332	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	V_{CC} = 4.75V, I_{OH} = -200μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	μA	V_{CC} = 5.25V, 0V ≤ V_{IN} ≤ 5.25V
I_{LO}	Output Leakage Current		10	μA	Chip Deselected· V_{OUT} = +0.4 V to V_{CC}
I_{CC}	Power Supply Current		100	mA	Output Unloaded, Chip Enabled V_{CC} = 5.25V, V_{IN} = V_{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	SY2332/33		Units	Test Conditions
		Min.	Max.		
t_{ACC}	Address Access Time		450	ns	Output load: 1 TTL load and 100pF
t_{CO}	Chip Select Delay		150	ns	Input Pulse Levels: 0.8 to 2.4V
t_{DF}	Chip Deselect Delay		150	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

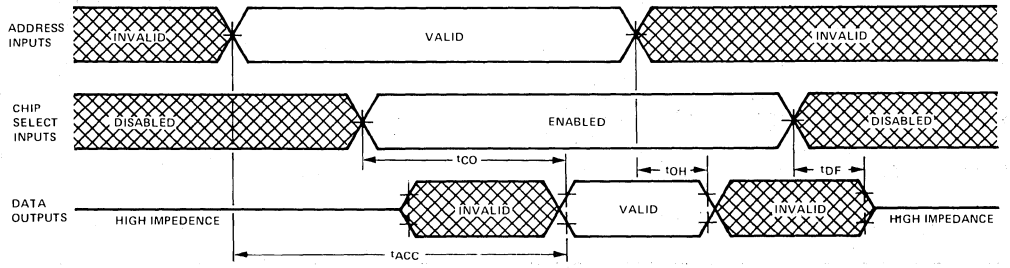
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch 2333 or 2332)
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank — pattern number to be assigned by Synertek
	30	$CS_2/\overline{CS_2}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"
	31	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O_8 or O_7) is the MSB and Output 1 (O_1 or O_0) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the inital input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2
	34-41	Output data for initial input address +3
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

Frames 7, 8	Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.
Frames 9 to 9+2* (Record Length) -1	Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).
Frames 9+2* (Record Length) to 9+2* (Record Length) +1	Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

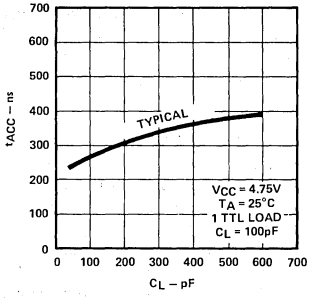
:0300010053F8ECC5

Send bit pattern data to the following special address:

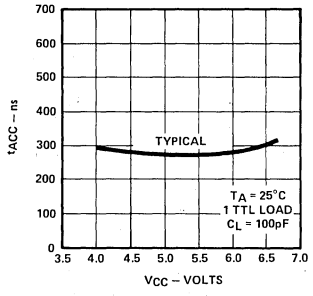
Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS

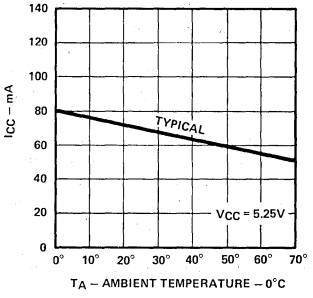
ACCESS TIME VS. CAPACITIVE LOAD



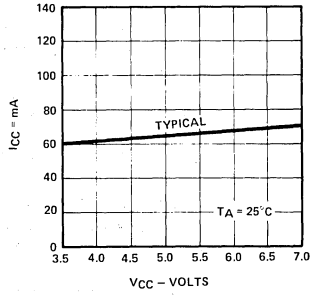
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

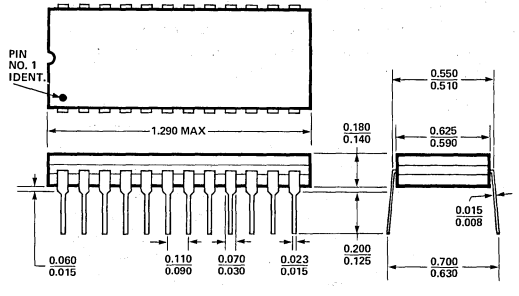


SUPPLY CURRENT VS. SUPPLY VOLTAGE

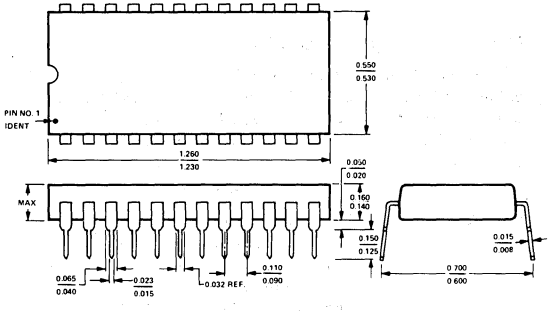


PACKAGING DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



4096 x 8 Static Read Only Memory

SY2332-3
SY2333-3

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- SY2333-2732 EPROM Pin Compatible
- 4096 x 8 Bit Organization
- Single +5 Volt Supply (±10%)
- Access Time—300ns (max)
- Totally Static Operation
- Completely TTL Compatible
- SY2332-2716 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- 2708/2716/2732 EPROMs Accepted as Program Data Inputs

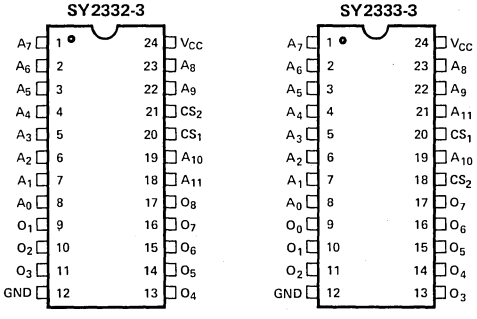
ROMs

The SY2332-3 and SY2333-3 high performance read only memories are organized 4096 words by 8 bits with access times of less than 300 ns. They are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

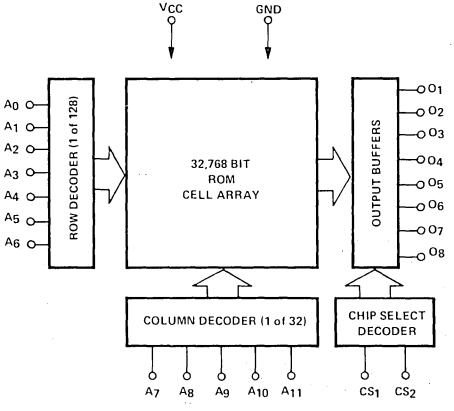
The SY2332-3 and SY2333-3 operate totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace 2716 or 2732 32K EPROMs, the SY2332-3 and SY2333-3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2333-3	Ceramic	300ns	0°C to +70°C
SYP2333-3	Plastic	300ns	0°C to +70°C
SYC2332-3	Ceramic	300ns	0°C to +70°C
SYP2332-3	Plastic	300ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	V_{CC} = 4.5V, I_{OH} = -400μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current		10	μA	Chip Deselected
					V_{OUT} = +0.4 V to V_{CC}
I_{CC}	Power Supply Current		100	mA	Output Unloaded, Chip Enabled
					V_{CC} = 5.5V, V_{IN} = V_{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	SY2332-3 and SY2333-3		Units	Test Conditions
		Min.	Max.		
t_{ACC}	Address Access Time		300	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		100	ns	and 100pF
t_{DF}	Chip Deselect Delay		100	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After	20		ns	Timing reference levels:
	Address Change Delay				Input: 1.5V
					Output: 0.8V and 2.0V

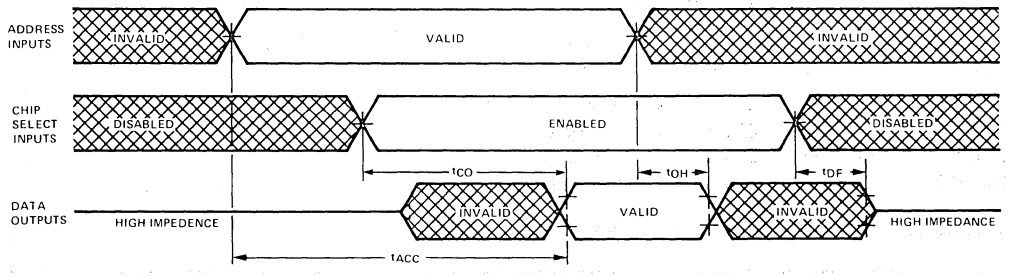
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch 2333 or 2332)
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_2/\overline{CS_2}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"
	31	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O_8 or O_7) is the MSB and Output 1 (O_1 or O_0) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the inital input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2
	34-41	Output data for initial input address +3
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

Frames 7, 8	Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.
Frames 9 to 9+2* (Record Length) -1	Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).
Frames 9+2* (Record Length) to 9+2* (Record Length) +1	Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

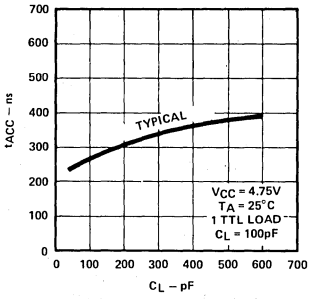
:0300010053F8ECC5

Send bit pattern data to the following special address:

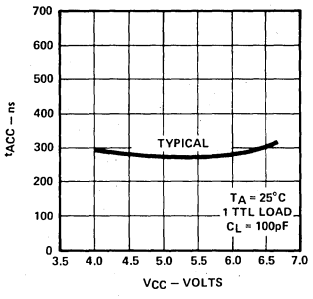
Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS

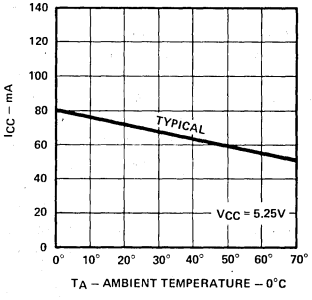
ACCESS TIME VS. CAPACITIVE LOAD



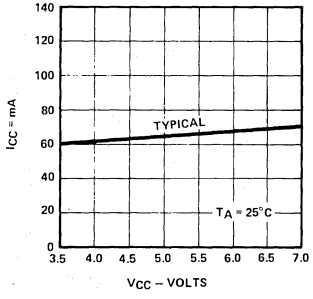
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

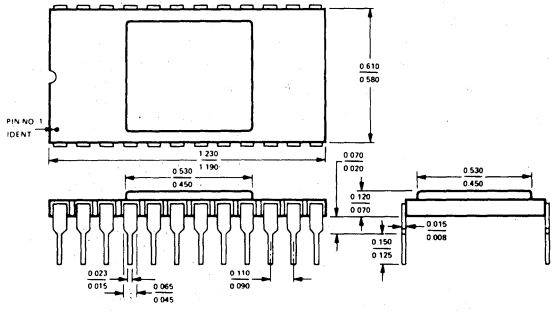


SUPPLY CURRENT VS. SUPPLY VOLTAGE



PACKAGE DIAGRAMS

CERAMIC PACKAGE



PLASTIC PACKAGE