ROM Selector Guide

Commercial: T_A = 0°C to +70°C

Part No.	Organization	Access Time Max. (ns)	Supply Current Max. (mA) Operating	Supply Current Max. (mA) Standby	Power Supply (Volts)	No. of Pins	Pin Compatible EPROM/PROM	Page
SY3308	1024 x 8	70	120	—	+5	24	82S181	2-32
SY2316A	2048 x 8	550	98	—	+5	24	—	2-3
SY2316B	2048 x 8	450	98	—	+5	24	2716	2-3
SY2316B-2	2048 x 8	200	98	—	+5	24	2716	2-7
SY2316B-3	2048 x 8	300	98	—	+5	24	2716	2-11
SY3316	2048 x 8	80	120	—	+5	24	82S191	2-36
SY3316A	2048 x 8	80	120	20	+5	24	82S191	2-36
SY2332	4096 x 8	450	100	—	+5	24	TMS2532	2-15
SY2332-3	4096 x 8	300	100	—	+5	24	TMS2532	2-19
SY2333	4096 x 8	450	100	—	+5	24	2732/A	2-15
SY2333-3	4096 x 8	300	100	—	+5	24	2732/A	2-19
SY2364	8192 x 8	450	100	—	+5	24	TMS2564	2-23
SY2364-2	8192 x 8	200	100	—	+5	24	TMS2564	2-23
SY2364-3	8192 x 8	300	100	—	+5	24	TMS2564	2-23
SY2364A	8192 x 8	450	100	12	+5	24	TMS2564	2-23
SY2364A-2	8192 x 8	200	100	12	+5	24	TMS2564	2-23
SY2364A-3	8192 x 8	300	100	12	+5	24	TMS2564	2-23
SY2365	8192 x 8	450	100	—	+5	28	2764	2-27
SY2365-2	8192 x 8	200	100	—	+5	28	2764	2-27
SY2365-3	8192 x 8	300	100	—	+5	28	2764	2-27
SY2365A	8192 x 8	450	100	12	+5	28	2764	2-27
SY2365A-2	8192 x 8	200	100	12	+5	28	2764	2-27
SY2365A-3	8192 x 8	300	100	12	+5	28	2764	2-27
SY23128[1]	16,384 x 8	200	100	10	+5	28	—	2-31

Military: -55°C to +125°C

SYM3316[1]	2048 x 8	100	150	—	+5	24	82S191	2-40
SYM3316A[1]	2048 x 8	100	150	30	+5	24	82S191	2-40

Note 1. To Be Announced.

2048 x 8 Static Read Only Memory

SY2316A/B

SYNERTEK
A SUBSIDIARY OF HONEYWELL

MEMORY PRODUCTS

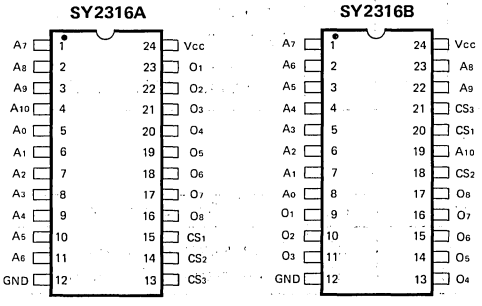
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time–550ns /450ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316A – Replacement for Intel 2316A
- SY2316B – Pin Compatible with 2716 EPROM
  – Replacement for Two 2708s

The SY2316A and SY2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

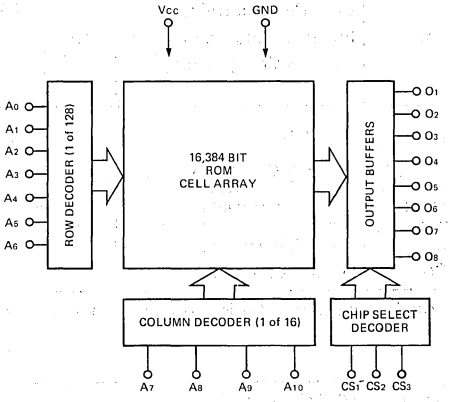
The SY2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace the 2716 16K EPROM, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2316A	Cerdip	550ns	0°C to +70°C
SYP2316A	Plastic	550ns	0°C to +70°C
SYD2316B	Cerdip	450ns	0°C to +70°C
SYP2316B	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	SY2316B		SY2316A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		450		550	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		120		300	ns	and 100 pf
t_{DF}	Chip Deselect Delay		100		150	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	10		20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.2V

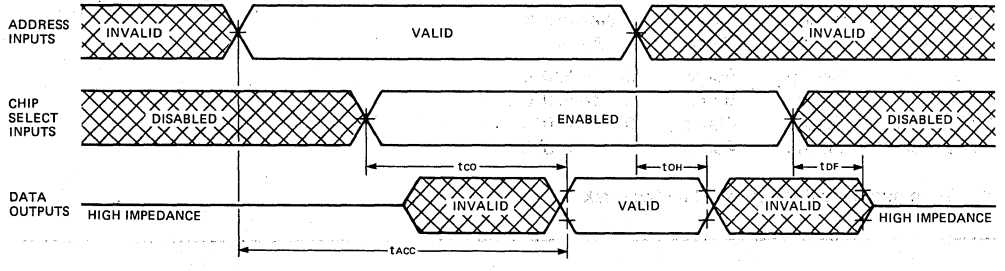
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316A" or "2316B")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

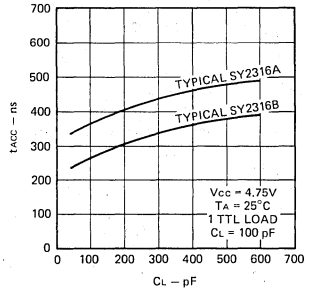
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

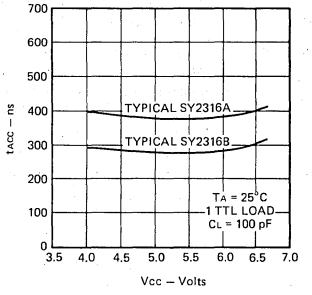
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

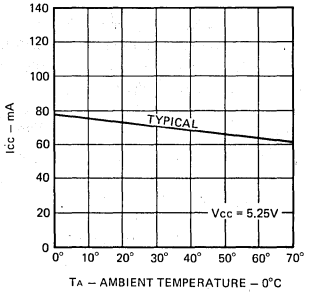
ACCESS TIME VS. CAPACITIVE LOAD



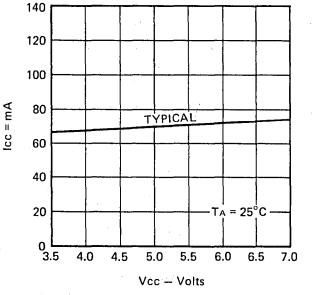
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

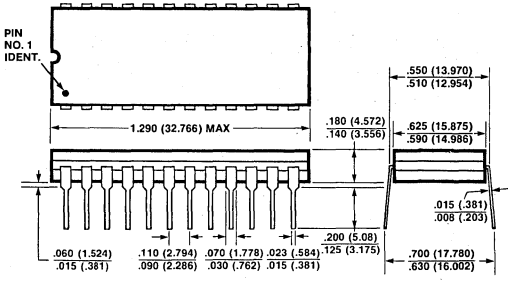


SUPPLY CURRENT VS. SUPPLY VOLTAGE

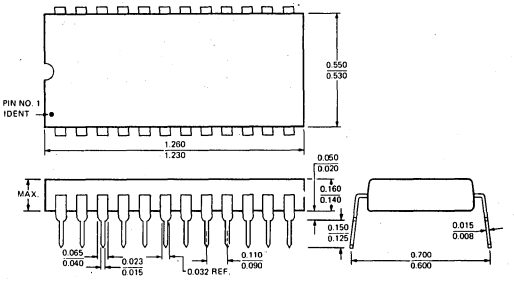


PACKAGE DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



2048x8 Static Read Only Memory

SY2316B-2

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

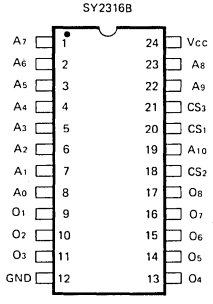
- Access Time—200ns (max.)
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- Metal Mask Programming
  —Two Week Prototype Turnaround
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316B — Pin Compatible with 2716 EPROM
  — Replacement for Two 2708s

The SY2316B-2 high performance Read Only Memory is organized 2048 words by 8 bits with an access time of less than 200ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

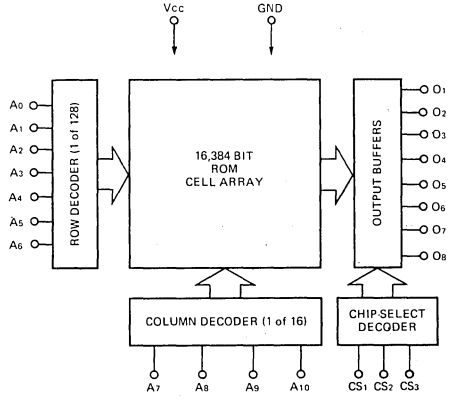
The SY2316B-2 operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The device offers three-state output buffers for memory expansion.

Designed to replace the 2716 16K EPROM, the SY2316B-2 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2316B-2	Cerdip	200ns	0°C to +70°C
SYP2316B-2	Plastic	200ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10° to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ Vin ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
Icc	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, Vin = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		200	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		100	ns	and 100 pF
t_{DF}	Chip Deselect Delay		100	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	10		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

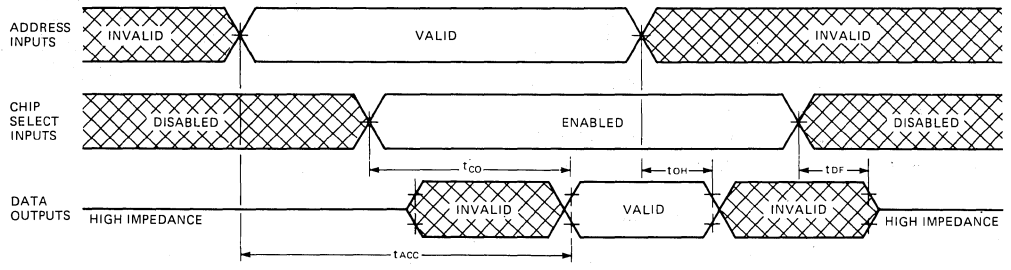
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316B-2")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

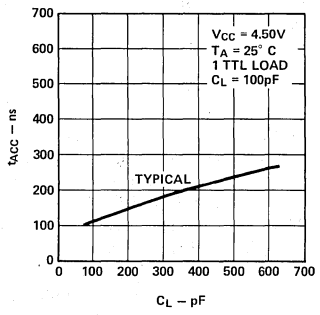
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

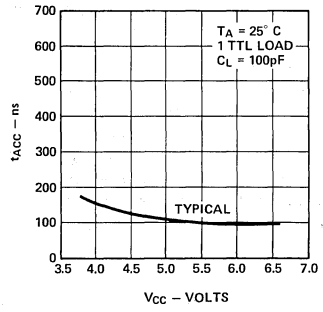
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

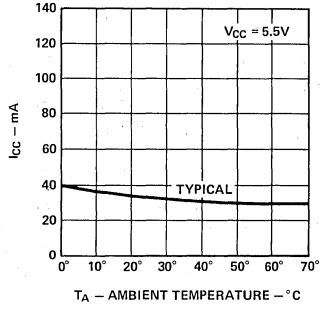
ACCESS TIME vs. CAPACITIVE LOAD



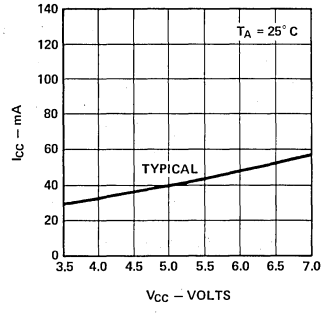
ACCESS TIME vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. AMBIENT TEMPERATURE

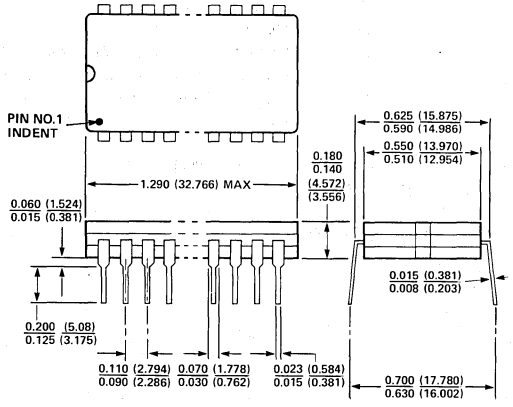


SUPPLY CURRENT vs. SUPPLY VOLTAGE

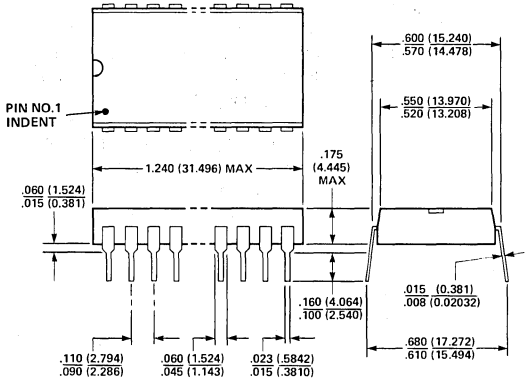


PACKAGING DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



2048 x 8 Static Read Only Memory

SY2316B-3

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- Access Time—300ns (max.)
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316B — Pin Compatible with 2716 EPROM
  — Replacement for Two 2708s

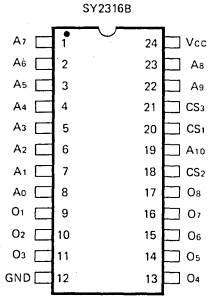
ROMs

The SY2316B-3 high performance Read Only Memory is organized 2048 words by 8 bits with an access time of less than 300 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

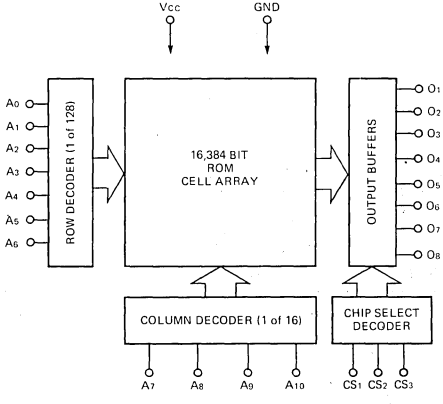
The SY2316B-3 operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The device offers three-state output buffers for memory expansion.

Designed to replace the 2716 16K EPROM, the SY2316B-3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2316B-3	Cerdip	300ns	0°C to +70°C
SYP2316B-3	Plastic	300ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10° to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		300	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		130	ns	and 100 pF
t_{DF}	Chip Deselect Delay		130	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

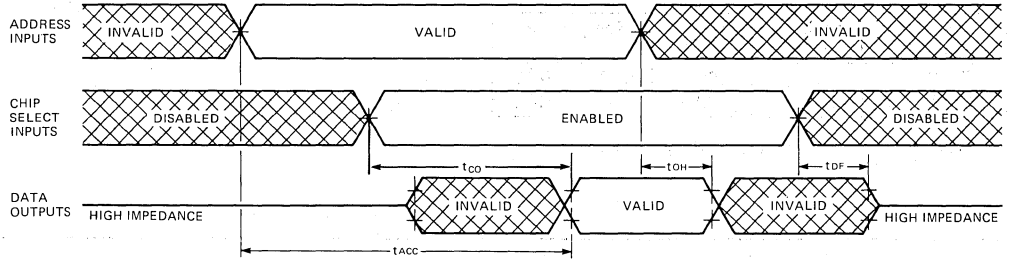
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316B-3")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

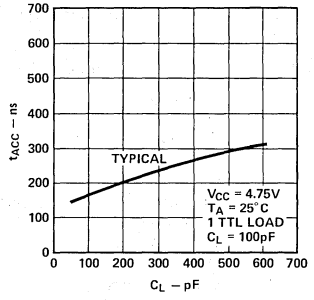
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

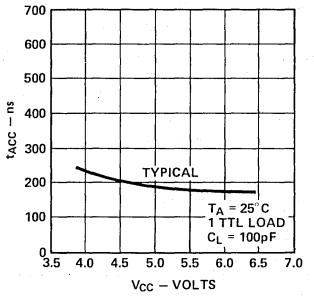
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

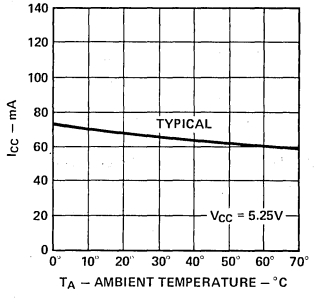
ACCESS TIME VS. CAPACITIVE LOAD



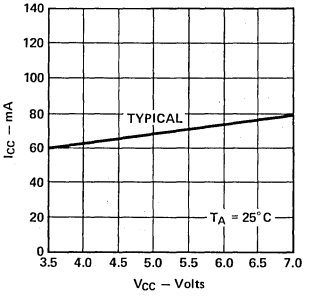
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

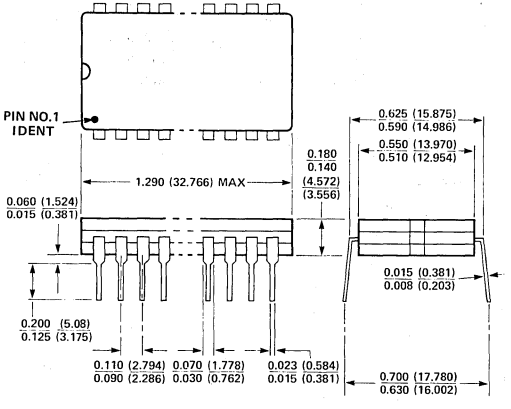


SUPPLY CURRENT VS. SUPPLY VOLTAGE



PACKAGING DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE